WHAT IS CLAIMED IS:

1. A via for use in a printed circuit board having a circuit, the via comprising:

a first interconnect; and

a second interconnect located about at least a portion of the first interconnect, the second interconnect being coaxial with the first interconnect and inductively coupled with the first interconnect, the second interconnect being connected to ground of the circuit.

2. The via of claim 1, wherein the first and second interconnects are substantially concentric.

3. The via of claim 2, wherein the first and second interconnects are cylinders in a single via hole.

4. The via of claim 1, wherein the second interconnect is operatively connected to at least two layers of the printed circuit board.

5. The via of claim 1, wherein a series ground inductance present in the signal return path is essentially canceled.

6. The via of claim 1, wherein the signal return has a voltage drop that approaches zero.

7. The via of claim 4, where the layers are located in a single printed circuit board.

8. The via of claim 4, where the layers are located in a monolithically integrated set of two or more printed circuit boards.

9. A printed circuit board comprising:

a plurality of vias according to claim 1.

10. A method of electrically interconnecting multiple layers on a printed circuit board to provide a common ground plane for a circuit, the method comprising:

connecting a first layer and at least a second layer to a via disposed in a through-hole of a printed circuit board, the via comprising a first interconnect and a second interconnect located about at least a portion of the first interconnect, the second interconnect being coaxial and substantially concentric with the first interconnect and inductively coupled with the first interconnect, the second interconnect being connected to ground of the circuit.

11. The method of claim 10, wherein at least two layers on a printed circuit board connect to the second interconnect to form one signal reference.